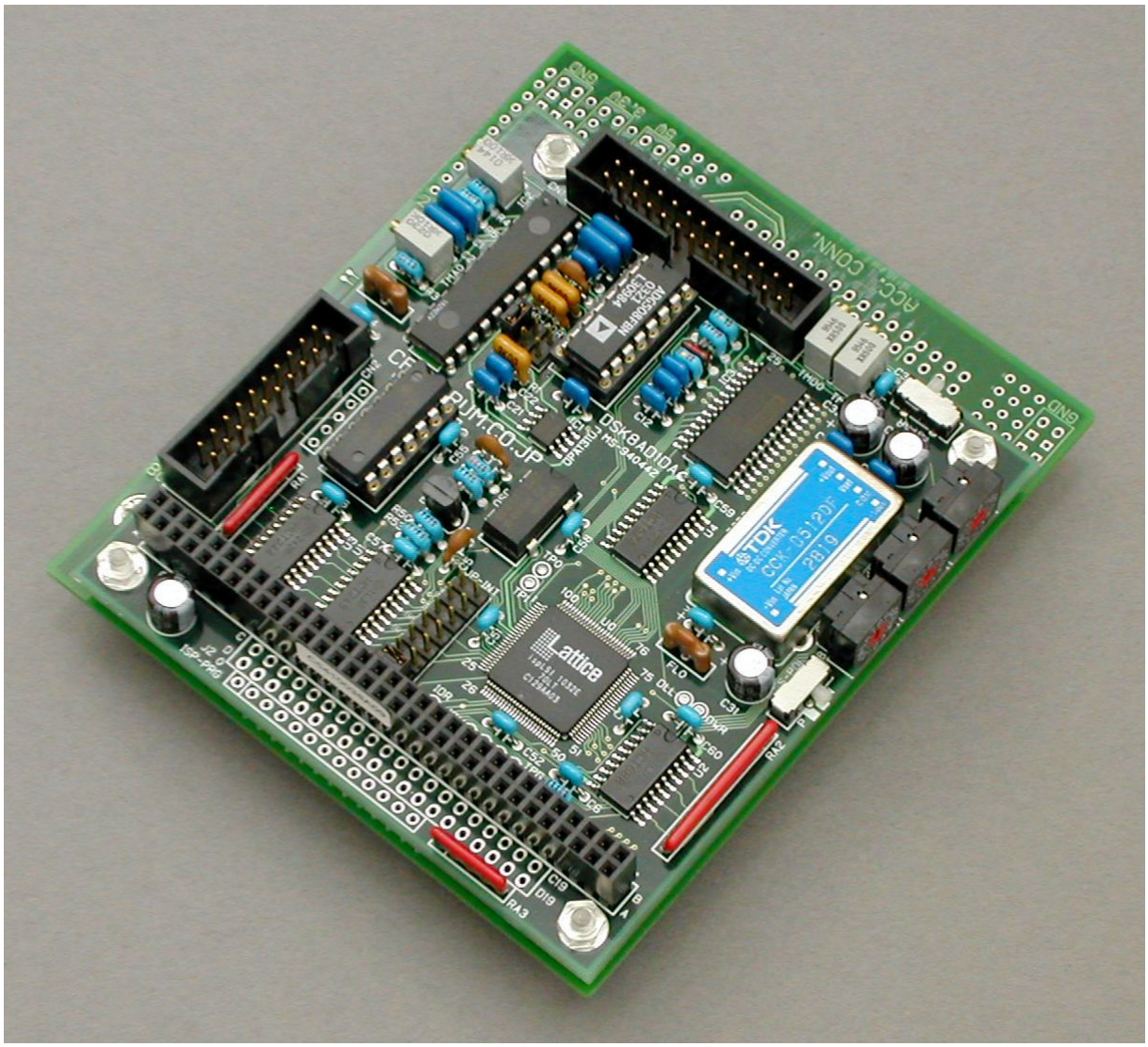
DSK8AD1DA

8ch A/D & 1ch D/A for DSK/EVM



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Rev.	date	remarks
1.1	2002.11.27	1st official release
1.2	2003.10.27	change D/A output voltage range, update board photos
1.3	2004.10.15	add sample programs for C6713 DSK

CAUTION!

DSK8AD1DA is designed for DSK/EVM with 5V tolerant EMIF not for 3.3V EMIF boards.

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DSK8AD1DA is designed for DSK/EVM with 5V tolerant EMIF not for 3.3V EMIF boards.

1. DSK8AD1DA hardware specification

1.1 A/D

A/D converter	ADS7800 (Burr-Brown/TI)
multiplexer	DG508
input channel number	8ch (SE : Single End)
input range	+/-10V, +/-5V, +/-2.5V (jumper selectable)
input impedance	100MΩ
corsstalk	typ 65dB
resolution	12bit
coding format	offset binary
non linearity	max +/-0.025%FS+/-1LSB
accuracy*	+/-0.105%FS
internal noise*	+/-1LSB
drift*	+/-25ppm/C.
conversion time	10us/channel

* typical measured value (not guarnteed)

1.2 D/A

D/A converter	DAC712 (Burr-Brown/TI)
output channel number	1ch (SE : Single End)
output range	+/-5V, 0:+5V (switch selectable)
output current	2mA (5kΩ/500pF load)
resolution	12bit
coding format	offset binary (bipolar)/straight binary (unipolar)
non linearity	max +/-0.0125%FS+/-0.5LSB
accuracy*	+/-0.05%FS
glitch*	15mV
drift*	+/-25ppm/C.
conversion time	10us

* typical measured value (not guarnteed)

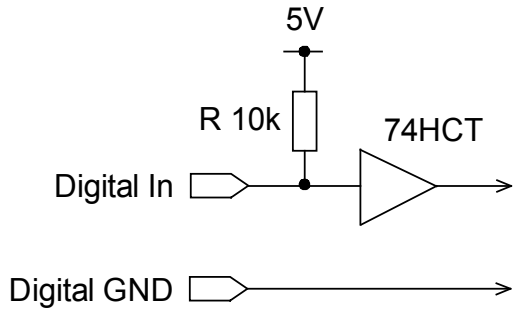
1.3 DIO

digital input	4bit
digital output	4bit

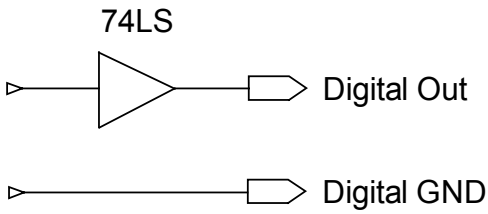
1.4 other

operating temperature	0C.-40C.
consumption current	600mA

1.5. DIO circuit



digital in



digital out

2. coding format

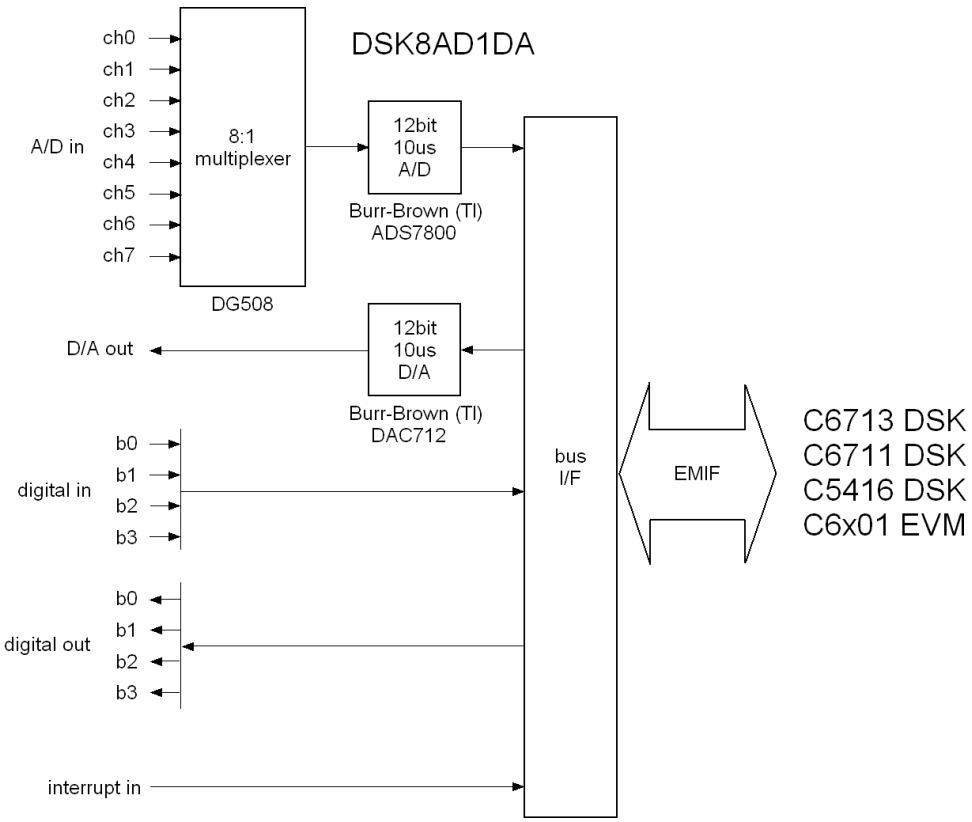
2.1 offset binary

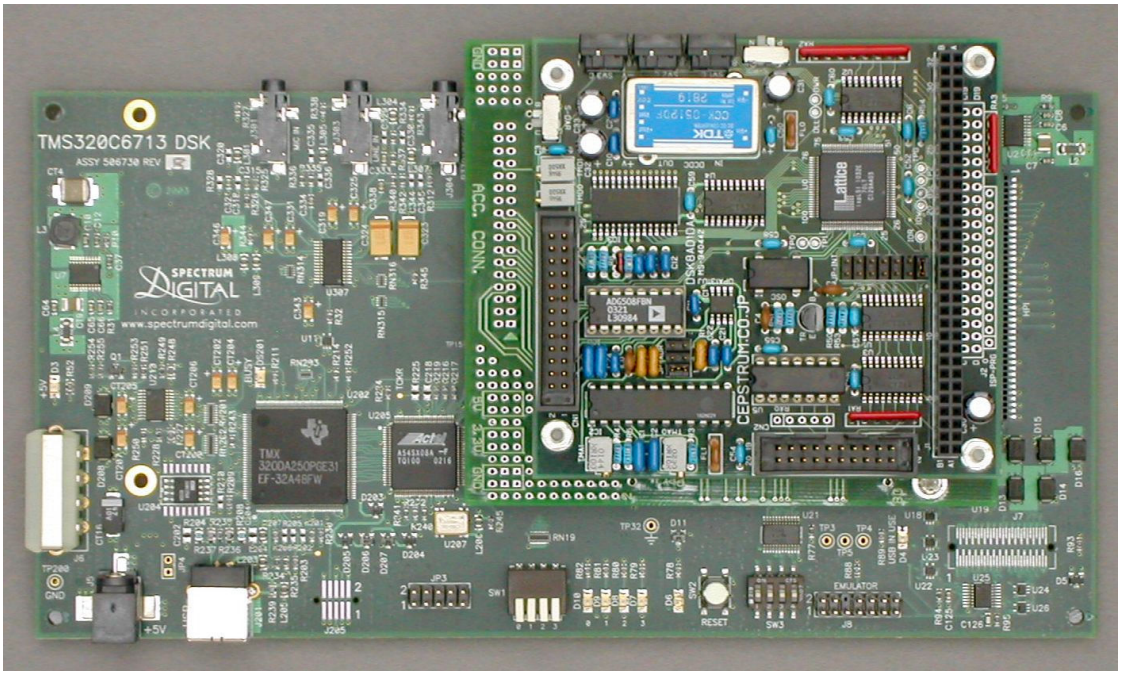
voltage / range			hex	decimal
+/-10V	+/-5V	+/-2.5V	value	value
+9.995V	+4.998V	+2.499V	0x0FFF	4095
:	:	:	:	:
:	:	:	:	:
0.0V	0.0V	0.0V	0x0800	2048
:	:	:	:	:
:	:	:	:	:
-10.0V	-5.0V	-2.5V	0x0000	0

2.2 straight binary

voltage / range		hex	decimal
0:+10V	0:+5V	value	value
+9.998V	+4.999V	0x0FFF	4095
:	:	:	:
:	:	:	:
+5.0V	+2.500V	0x0800	2048
:	:	:	:
:	:	:	:
0.0V	0.0V	0x0000	0

3. DSK8AD1DA block diagram

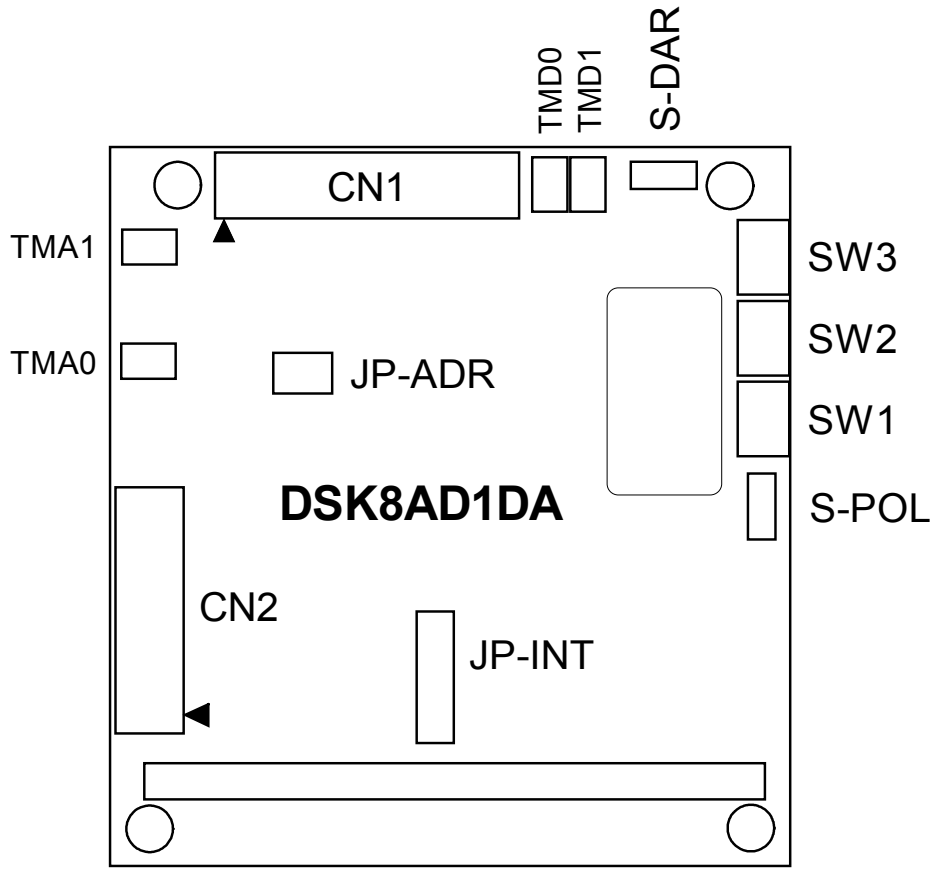




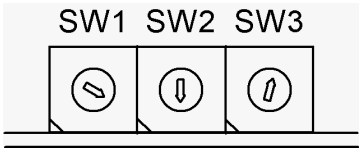
5DSK8AD1DA on C6713 DSK

4. hardware setting

4.1 DSK8AD1DA board layout



4.2 SW1, SW2, SW3 board address SW (on DSK/EVM EMIF)

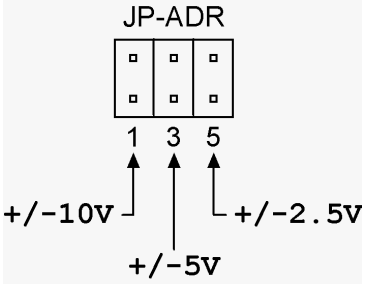


side view

SW	EMIF address bit
SW1	EA14 - EA17
SW2	EA10 - EA13
SW3	EA6 - EA9

DSK8AD1DA is located on CE2 space of EMIF

4.3 JP-ADR A/D input range jumper

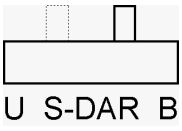


jumper	range
1	+/-10V
3	+/-5V
5	+/-2.5V

4.4 TMA0 A/D input DC offset trim

4.5 TMA1 A/D input gain trim

4.6 S-DAR D/A output range switch

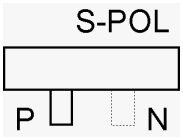


position	rage
U	unipolar (0:+5V)
B	bipolar (+/-5V)

4.7 TMD0 D/A output DC offset trim

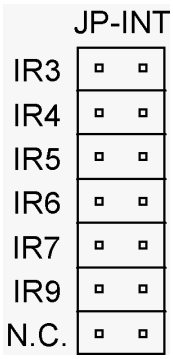
4.8 TMD1 D/A output gain trim

4.9 S-POL digital output polarity switch



position	polarity
P	positive
N	negative

4.10 JP-INT interrupt routing jumper



jumper	DSK/EVM interrupt pin
IR3	EXT_INT4
IR4	EXT_INT5
IR5	EXT_INT6
IR6	N.C.
IR7	N.C.
IR9	N.C.
N.C.	N.C.

5. connector pinout

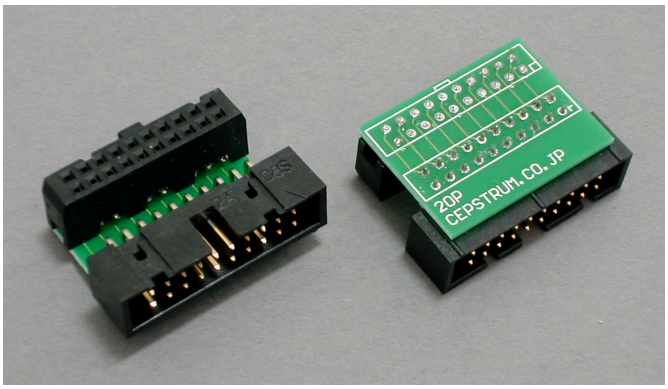
5.1 CN1 A/D· D/A input/output

	signal name	pin No.	CN1	pin No.	signal name	
ch0 input	CH0	1	▶ O O	2	AG	analog ground
ch1 input	CH1	3	O O	4	AG	analog ground
ch2 input	CH2	5	O O	6	AG	analog ground
ch3 input	CH3	7	O O	8	AG	analog ground
ch4 input	CH4	9	O O	10	AG	analog ground
ch5 input	CH5	11	O O	12	AG	analog ground
ch6 input	CH6	13	O O	14	AG	analog ground
ch7 input	CH7	15	O O	16	AG	analog ground
		17	O O	18		
		19	O O	20		
		21	O O	22		
output	DA	23	O O	24	AG	analog ground
		25	O O	26		

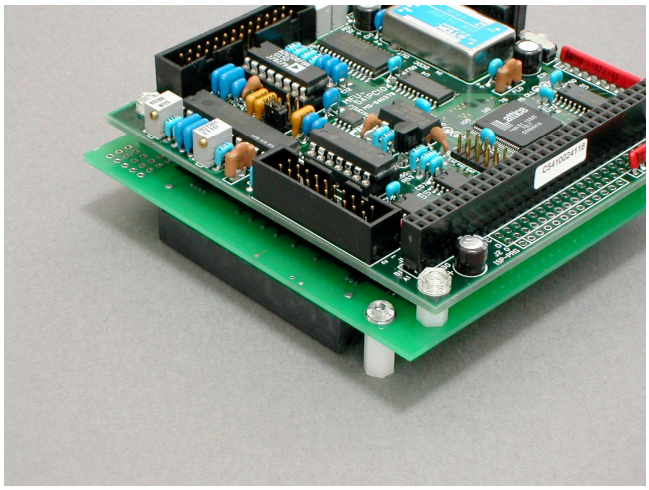
5.2 CN2 digital input/output & interrupt input

	signal name	pin No.	CN2	pin No.	signal name	
b0 input	DI0	1	▶ O O	2	DG	digital ground
b1 input	DI1	3	O O	4	DG	digital ground
b2 input	DI2	5	O O	6	DG	digital ground
b3 input	DI3	7	O O	8	DG	digital ground
b0 output	DO0	9	O O	10	DG	digital ground
b1 output	DO1	11	O O	12	DG	digital ground
b2 output	DO2	13	O O	14	DG	digital ground
b3 output	DO3	15	O O	16	DG	digital ground
intr.input	INT	17	O O	18	DG	digital ground
+5V output	VDD	19	O O	20	DG	digital ground

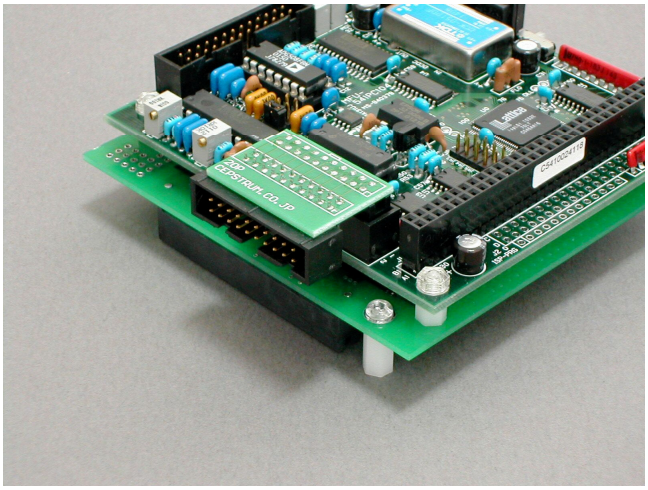
5.3 extension adaptor(option for stacked board)



extension adaptor (20pin)



DSK8AD1DA



DSK8AD1DA with extension adaptor on CN2

5.4 extension adapter pinout for CN1

A/D･ D/A input/output

	signal name	Pin No.	ext. (CN1)	pin No.	signal name	
		1	O O	2		
output	DA	3	O O	4	AG	analog ground
		5	O O	6		
		7	O O	8		
		9	O O	10		
ch7 input	CH7	11	O O	12	AG	analog ground
ch6 input	CH6	13	O O	14	AG	analog ground
ch5 input	CH5	15	O O	16	AG	analog ground
ch4 input	CH4	17	O O	18	AG	analog ground
ch3 input	CH3	19	O O	20	AG	analog ground
ch2 input	CH2	21	O O	22	AG	analog ground
ch1 input	CH1	23	O O	24	AG	analog ground
ch0 input	CH0	25	O O	26	AG	analog ground

5.5 extension adapter pinout for CN2

digital input/output & interrupt input

	signal name	pin No.	ext. (CN2)	pin No.	signal name	
+5v	VDD	1	O O	2	DG	digital ground
intr.input	INT	3	O O	4	DG	digital ground
b3 output	DO3	5	O O	6	DG	digital ground
b2 output	DO2	7	O O	8	DG	digital ground
b1 output	DO1	9	O O	10	DG	digital ground
b0 output	DO0	11	O O	12	DG	digital ground
b3 input	DI3	13	O O	14	DG	digital ground
b2 input	DI2	15	O O	16	DG	digital ground
b1 input	DI1	17	O O	18	DG	digital ground
b0 input	DI0	19	O O	20	DG	digital ground

6. control register map & setting

6.1 register map

EMIF base address (EA2-EA5)	register write	page
0x00	A/D start	13
0x01	(not used)	--
0x02	set interrupt mode	13
0x03	digital out	14
0x04	(not used)	--
0x05	(not used)	--
0x06	D/A write (b0-b7)	13
0x07	D/A write (b8-b11)	13

EMIF base address (EA2-EA5)	register read	page
0x00	A/D read (b0-b7)	14
0x01	A/D read (b8-b11)	14
0x02	read status	14
0x03	digital in	14
0x04	(not used)	--
0x05	(not used)	--
0x06	(not used)	--
0x07	board reset	13

* upper EMIF address (EA6-EA17) is selected by SW1-SW3
* DSK8AD1DA is located on CE2 space of EMIF
* register width = 8bit

6.2 board reset +0x07 read

bit	definition	reset value
b0-b7	DSK8AD1DA board ID (0x1D)	0x1D

6.3 set interrupt mode +0x02 write

bit	definition	vlaue=1	value=0	reset value
b0-b2	(not used)	---	---	0
b3	clear interrupt flag	clear	no effect	0
b4-b5	(not used)	---	---	0
b6	interrupt signal edge	positive	negative	0
b7	interrupt enable	enable	disable	0

6.4 D/A write +0x06, +0x07 write

example:

```
outp(BASE+0x06, d1);
outp(BASE+0x07, d2);
```

data	bit	definition
d1	b0-b7	D/A data bit0-bit7
d2	b0-b3	D/A data bit8-bit11
d2	b4-b7	(not used)

6.5 A/D start +0x00 write

bit	definition	reset value
b0-b2	input channel number (0x00-0x07)	0
b3-b7	(not used)	0

6.6 read status +0x02 read

bit	definition	value=1	value=0	reset value
b0	A/D flag	converting	conversion end	0
b1-b2	(not used)	---	---	0
b3	interrupt flag	occur	not occur	0
b4-b5	(not used)	---	---	0
b6	interrupt status	(current interrupt pin status)		0
b7	(not used)	---	---	0

6.7 A/D read +0x00, +0x01 read

example:

```
a1=inp(BASE+0x00);
a2=inp(BASE+0x01);
```

data	bit	definition
a1	b0-b7	A/D data bit0-bit7
a2	b0-b3	A/D data bit8-bit11
a2	b4-b7	(not used)

6.8 digital out +0x03 write

bit	definition
b0-b3	4bit digital out data
b4-b7	(not used)

output data is latched

6.9 digital in +0x03 read

bit	definition
b0-b3	4bit digital in data
b4-b7	(not used)

7. library & software for DSK8AD1DA

7.1 raw.c (A/D, D/A, DO sample program)

```
// DSK & DSK8AD1DA
// loopback test program without library
//
// DSK8AD1DA A/D ch0 in --> DSK8AD1DA D/A out
//
// DSK8AD1DA setup
//   SW1  =1
//   SW2  =3
//   SW3  =7
//   S-DAR=B (bipolar)

#include "c6713dsk.h"
//#include "c671dsk.h"

#define  UCHAR    unsigned char
#define  IOBASE   0xa0001370     // SW1="1", SW2="3", SW3="7"

void main(void) {
  int  temp;

  CSR=0x100;                                    // disable all interrupts
  IER=IER|0x02;                                 // enable NMI
  CSR=CSR|1;                                    // enable interrupt (global)

  *(unsigned int *)EMIF_CE2=0xfa3fe80f;         // EMIF CE2 configuration
  temp=*(UCHAR *)(IOBASE+7);                    // reset DSK8AD1DA

  while(1) {                                    // forever loop
    *(UCHAR *)(IOBASE+3)=0x07;                  // digital out (hi)
    *(UCHAR *)IOBASE=0;                         // A/D start (ch0)
    while ((*(UCHAR *)(IOBASE+2))&0x01!=0) {    // wait until conversion end
      ;
    }
    temp=*(UCHAR *)IOBASE;                          // A/D read (LO)
    temp=temp|(((*(UCHAR *)(IOBASE+1))&0x0f)<<8);  // A/D read (HI)
    *(UCHAR *)(IOBASE+3)=0;                         // digital out (lo)
    /* something to do here */
    *(UCHAR *)(IOBASE+6)=temp&0x00ff;               // D/A out (LO)
    *(UCHAR *)(IOBASE+7)=(temp&0x0f00)>>8;          // D/A out (HI)
  }

}
```

7.2 support library for C6711 DSK

7.2.1 library files

```
dsk8ad1da.h      header file
dsk8ad1da.c      source code
dsk8ad1da.obj    object file
dsk8ad1da.lib    library file
```

7.2.1 header file list (dsk8ad1da.h)

```
001: // DSK + DSK8AD1DA (little endian)
002:
003: int           init8a1d(unsigned short);
004: void          do8a1d(unsigned char);
005: unsigned char di8a1d(void);
006: void          da8a1d(short);
007: short         ad8a1d(unsigned char);
008: void          mult_ad8a1d(unsigned char, short[]);
009: void          set_interrupt8a1d(unsigned char);
010: unsigned char read_status8a1d(void);
```

7.3 library functions

7.3.1 init8a1d board initialize

```
int init8a1d(unsigned short sw123);
  sw123        : board address (SW1, SW2, SW3 value in hex)
  return value : 0 (board exists), 1 (no board)
```

7.3.2 do8a1d 4bit digital out

```
void do8a1d(unsigned char do_data);
  do_data : 4bit output data
```

7.3.3 di8a1d 4bit digital in

```
unsigned char di8a1d(void);
  return value : 4bit input data
```

7.3.4 da8a1d D/A (bipolar output)

```
void da8a1d(short da_data);
  da_data : 12bit D/A data
```

7.3.5 ad8a1d A/D (single channel)

```
short ad8a1d(unsigned char channel);
  channel      : A/D channel number (0-7)
  return value : 12bit A/D data
```

7.3.6 mult_ad8a1d A/D (multi channel)

```
void mult_ad8a1d(unsigned char channel, short ad_data[]);
  channel   : A/D end channel number (0-7)
  ad_data[] : A/D data
```

7.3.7 set_interrupt8a1d set interrupt mode

```
void set_interrupt8a1d(unsigned char x);
  x : interrupt mode data
  write interrupt mode register   (register address)=BASE+0x02
```

7.3.8 read_status8a1d read status (read status register)

```
unsigned char read_status8a1d(void);
  return value : status data
  read status register   (register address)=BASE+0x02
```

7.4 sample0.c (A/D, D/A, DO sample program)

```
// DSK & DSK8AD1DA
// loopback test program
//
// DSK8AD1DA A/D ch0 in --> DSK8AD1DA D/A out
//
// DSK8AD1DA setup
//   SW1  =1
//   SW2  =3
//   SW3  =7
//   S-DAR=B (bipolar)

#include "c6713dsk.h"
//#include "c6711dsk.h"
#include "dsk8ad1da.h"

#define  IOBASE8AD1DA  0x137    // SW1="1", SW2="3", SW3="7"

void main(void)

  int  temp;

  CSR=0x100;                    // disable all interrupts
  IER=IER|0x02;                 // enable NMI
  CSR=CSR|1;                    // enable interrupt (global)

  temp=init8a1d(IOBASE8AD1DA);  // initialize DSK8AD1DA

  while(1) {                    // forever loop
    do8a1d(0x07);               // digital out (hi)
    temp=ad8a1d(0);             // A/D in (ch0)
    do8a1d(0x00);               // digital out (lo)
    /* something to do here */
    da8a1d(temp);               // D/A out
  }

}
```

7.5 sample programs in CD-R

directory	description
dsk8ad1da	library for C6711 DSK, C6713 DSK
raw	raw A/D, D/A, DO sample program without library
sample0basic	simple sample program
sample1loop	free running loop back A/D, D/A
sample3timer	timer interrupt A/D, D/A (fs=10kHz)
sample4mult	multi channel A/D
sample5ext	external clock driven A/D, D/A

■ 本製品は 5V 耐入力の EMIF bus を有する DSK/EVM に適合します.
2005 年現在 TI より販売されている DSK/EVM はいずれも 5V 耐入力ですが, 将来新たに販売される DSK/EVM が 5V 耐入力である保証は無いことにご注意下さい.
本製品を 3.3V EMIF bus （5V 入力不可）の DSK/EVM と組み合わせて使用した場合, DSK/EVM を損傷する可能性があります.

■ C6711 DSK, C6713 DSK と組み合わせて本製品を使用される場合は, CD-R に収録されているライブラリ（dsk8ad1da.obj, dsk8ad1da.lib）をご利用下さい.
ライブラリを用いたサンプルプログラムも CD-R に収録されています.

■ C6711 DSK, C6713 DSK 以外の DSK/EVM 用のプログラムを作成される場合は, ライブラリのソース dsk8ad1da.c を参考にして下さい. （CD-R に収録）
CD-R に収録されているプログラムを使用される場合は, いったんファイルをハードディスクにコピーしてから, read only（読み取り専用）の属性をはずしてからご利用ください. （read only のままではプログラムの修正・コンパイル・ビルドは出来ません）

■ CD-R 収録のプログラムは CCS (Code Composer Studio) Ver.2.1 を用いて作成しています. 旧版の CCS Ver.1.x でコンパイル・ビルドをする場合は, CCS Ver.1.x でプロジェクトを作成しなおして下さい. （Ver.2.x と Ver.1.x とはプロジェクト・ファイルのフォーマットが異なっています）

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